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EXAMINER	
DILLER, JESSE DAVID	

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,682	ELBOIM ET AL.	
	Examiner	Art Unit	
	Jesse Diller	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Examiner acknowledges receipt of the amendment in response to the office action dated 03/28/2006, which amendment was received 05/12/2006. At this point, claims 1, 8, 10, 15, and 20 have been amended, claims 5 and 22 have been cancelled, and claims 23-25 have been added. Thus, claims 1-4, 6-21, and 23-25 are now pending in the application.

2. The indicated allowability of claims 14, 17-19 is withdrawn in view of the newly discovered reference(s) to Tomashima. Rejections based on the newly cited reference(s) follow. **As these rejections were not necessitated by amendment, this action is Non-Final.**

Response to Arguments

3. **Applicant's arguments filed with respect to the rejections of claims** 1-10 by Kao **are moot in view of the new rejection below.**

4. **Applicant's arguments filed with respect to the 35 USC § 102 rejections of claims 11-13, 15-16 by Bonaccio in view of Kao have been fully considered but they are not persuasive.** Applicants contend that Bonaccio does not teach the identification of a subset of test data that correspond to a subset of register having correct default values. However, please see the last bullet of Par. 25 of the prior office action and Pars. 6-7 of Bonaccio. Values for the configuration registers come from one

of several places,, the default power-on value (par. 6, lines 1-5), the POR reset memory (14, Fig. 2), or the NV memory 140. The configuration sets (142, Fig. 2) are complete configurations; for a configuration set to include values for less than all of the registers must inherently mean that the power-on default values are the correct ones. For the configuration sets to be determined and correctly functional, the registers which do and do not contain the correct POVs must be determined. Therefore, the rejection is seen to be correct.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-2 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Kao et al., US 6,119,192.**

6. **As for claim 1, Kao teaches:**

- a non-volatile memory storing information to load a plurality of configuration registers of a device (addresses 0-5n, Fig. 5), wherein
- the information includes a plurality of address information and a plurality of data corresponding to the plurality of address information (see address information 0, 5, 5m, 5n and data information 1-4, 6, 5m+1-5m+4, Fig. 5),
- each of the plurality of address information identifying at least one of the plurality of configuration registers to which a corresponding data should be written (see Fig. 5; the address information is an index referring to the appropriate register; see 365, Fig. 3).
- the non-volatile memory has a memory size less than a memory size sufficient to fill all the configuration registers (memory stores values for only some (less than all) configuration registers; see Col. 3, lines 10-15; Claim 2)

7. **As for claim 2, Kao additionally teaches:**

- The non-volatile memory is an Electrically Erasable Programmable Read-only Memory (See Col. 3, line 43) and
- the configuration registers are used to define parameters for communication between the device and at least one other device (See Cols 1-2).

8. **As for claim 6, Kao additionally teaches:**

- a block of control logic coupled to the memory, the block of control logic to write the plurality of data to the plurality of configuration registers according to the plurality of address information (see 205, Fig. 2; for multiple logic blocks which control the loading).

9. **As for claim 7, Kao additionally teaches:**

- the plurality of configuration registers are to be loaded during an initialization of the device (Col. 3, lines 27-35: section b; the loading happens on startup).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Bonaccia et al., US 2004/0143715.**

11. **As for claims 3-4, Kao teaches** the limitations of claim 1, as above. Kao does not teach, however, that the device is an analog communication device, as does claim 3 or that the device is a processor, memory controller, or Ethernet controller, as does claim 4.

12. Bonaccio teaches a system and method for loading sets of configuration registers from a non-volatile memory. He teaches, in Pars. 4 and 20-21, that many Ics allow the user to configure the circuit using configuration registers. He cites several examples, such as in HD read channel controllers or microprocessors in Par. 4 and analog communications circuits in the last lines of Par. 6. Further, in Pars. 20-21, he teaches that the methods of loading configuration registers may be applied not only to ICs such as hard disk channel controllers, but to any IC configured by registers.

13. Kao and Bonaccio are analogous art,because they are from the same area of endeavor, namely systems for setting configuration registers.

14. At the time of the invention it would have been obvious to use the system of setting configuration registers as taught by Kao in an environment such as a microprocessor or analog communication circuit.

15. The motivation for doing so is taught by Bonaccio in Par. 4, namely that using programmable registers is widely used in many ICs to allow the user to configure the function of the chip. Further, Kao teaches in Col. 3, lines 60-66 that his invention would be beneficially used in many systems where it is desirable to configure a peripheral device in an expedited manner prior to a normal system initialization procedure.

16. Therefore, it would have been obvious to use the register loading process of Kao in different environments, thereby obtaining the invention of claims 3-4.

17. **Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Bonaccia et al., US 2004/0143715 and Tomashima et al., US 6,480,946 B1.**

18. **As for claim 8, Kao teaches:**

- loading the plurality of configuration registers (365, Fig. 3; see also Col. 3, lines 27-35: section b) according to information stored in a non-volatile memory (160, Fig. 1), wherein
- the information in a memory includes a plurality of address information and a plurality of data corresponding to the plurality of address information, each of the plurality of address information identifying at least one of the plurality of to which a corresponding data should be written (see address information 0, 5, 5m, 5n

and data information 1-4, 6, 5m+1-5m+4, Fig. 5; see also Fig. 5; the address information is an index referring to the appropriate register; see 365, Fig. 3).

19. Kao does not teach, however,

- resetting each of a plurality of configuration registers of a device to a register default data value before loading the registers, or
- repeating resetting and loading to repeat a multi-stage test data loading process with subsequent test information stored in the non-volatile memory.

20. **Bonaccio teaches** a system and method for loading sets of configuration registers from a non-volatile memory. He teaches, in Par. 6, that configuration values may come from several sources. Usually, the registers are made up of latches which are designed to be reliably reset to a specific state when power is first applied. He also teaches that rather than hard-wiring these values, a POR value memory, 14, Fig. 1, may be used to reset each of the configuration registers to a default value which can be changed and subsequently reset from the non-volatile memory. Bonaccio also teaches that the memory includes a plurality of sets of configurations (see 142, Fig. 2).

21. Kao and Bonaccio are analogous art,because they are from the same area of endeavor, namely systems for setting configuration registers.

22. At the time of the invention it would have been obvious to modify the system of Kao to use the Power-on value memory taught by Bonnacio to reset the registers to a default value on power-up.

23. The motivation for doing so is taught by Bonaccio in Pars 6-7, namely that sometimes the default values are correct, and sometimes they need to be changed.

Therefore, it would have been obvious to use the default register value of Bonaccio in the system of Kao.

24. **Tomishima teaches a** system for setting the timing of memory devices, which includes setting configuration registers with various delay and voltage settings. See Fig. 43, where certain configuration settings are applied, and the system is tested. If the results are not as desired, the configuration is changed and the test is repeated.

25. Tomashima and the system of Bonaccio and Kao are analogous because they are both from the same area of endeavor, namely configuration systems.

26. At the time of the invention, it would have been obvious to apply the method of Tomashima to the system of Bonaccio and Kao, so that each configuration set 142 contains different configuration settings. Each set can be loaded, and the system tested. If the configuration results in certain registers not at desired values (i.e., S4:NO, Fig. 43 of Tomashima), the next configuration set may be loaded and the test rerun.

27. The motivation is that this allows the automated determination of the correct values for the configuration registers (Col. 37, lines 40-45 of Tomashima), and because the configuration sets may contain values for less than all of the registers, the loading time and storage required can be minimized, and thereby obtaining the system of claim 8.

28. **As for claim 9, Kao also teaches:**

- The loading occurs during the initialization of a communication controller device (see 150-160, Fig. 1 and Fig. 2; the system is a PCI communications bus controller).

29. **As for claim 10, Kao also teaches:**

- updating the information stored in the non-volatile memory with a second plurality of address information and second a plurality of data corresponding to the second plurality of address information, each of the second plurality of address information identifying at least one of the plurality of to which a corresponding one of the second plurality of data should be written (Col. 7, lines 10-25).

30. **Claim 11-13, 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Bonaccio in view of Kao.**

31. **As for claim 11, Bonaccio discloses:**

- selecting a desired configuration of a device, the desired configuration associated with desired data to be stored in a plurality of registers of the device; (see Par. 9; also Par. 29, first 5 lines; also first half of Par. 27; the start register designates a configuration set)
- storing test information associated with the desired configuration in a memory (Par. 29, Fig. 1; the configuration sets are test information associated with various configurations);
- resetting each of the plurality of registers to a register default data value (Par. 6);
- loading at least two of the plurality of registers according to the test information (Par. 32),
- identifying a subset of the plurality of test data that correspond to a subset of the plurality of registers having default data values equal to desired data for achieving the desired configuration *prior* to loading (*NOTE: see section entitled*

Claim Rejections – 35 USC § 112. See Fig. 1, Par. 23; loading a single set may load less than all of the registers. In other words, a desired configuration may identify a few registers to be updated; for the rest, the default value is the correct one).

32. Bonaccio does not expressly disclose that

- the test information includes a plurality of test address information and a plurality of test data corresponding to the plurality of test address information, each of the plurality of test address information identifying at least one of the plurality of registers to which a corresponding test data should be written

33. Instead, Bonaccio teaches that the configuration sets stored in the non-volatile memory contain only data; an address generator, a start register, and a duration register (144, 150B, 150C, Fig. 2) are used to generate the addresses which correspond to the data and to the target register.

34. Kao discloses a similar system and method of loading configuration registers, where initialization data is stored in a non-volatile memory and subsequently loaded into the registers during system startup. In the system of Kao, an address generator is not used. Instead, the register address is stored in the memory along with the data to =be stored. See Fig. 5.

35. Bonaccio and Kao are analogous art because they are from the same area of endeavor, namely systems for loading configuration registers.

36. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Bonaccio by replacing the address generator and address registers 150b,c with the address+data system of Kao.

37. The motivation for doing so is taught by Kao on Col. 3, lines 9-15, namely that this increases system efficiency and speed. Because the address is already stored in the memory, the address generator does not need to generate an address; it can simply be loaded with the data.

38. Therefore, it would have been obvious to combine Kao with Bonaccio for the benefit of increased circuit simplicity and speed, to obtain the invention as specified in claim 11, 15.

39. **As for claim 12-13, the system of Kao and Bonaccio teaches:**

- wherein the test information includes a word of register address information and corresponding register data words for each one of the plurality of registers (see Fig. 5, Kao; the test information includes a register address and corresponding data; see also Bonaccio, last half of Par. 23).

40. **As for claim 16, the system of Kao and Bonaccio teaches:**

- resetting and loading occur during initialization of a communication controller device (see Bonaccio, ; Kao, Col. 3, lines 27-35: section b; the loading happens on startup).

41. **Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Bonaccio and Cohen, US 5,737,524.**

42. **Kao teaches**

- a plurality of configuration registers of a device (210, Fig. 1),
- a non-volatile memory storing information to load a plurality of configuration registers of a device (addresses 0-5n, Fig. 5), wherein
- the information includes a plurality of address information and a plurality of data corresponding to the plurality of address information (see, for instance, address information 0, 5, 5m, 5n and data information 1-4, 6, 5m+1-5m+4, Fig. 5),
- each of the plurality of address information identifying at least one of the plurality of configuration registers to which a corresponding data should be written (see Fig. 5; the address information is an index referring to the appropriate register; see 365, Fig. 3).
- a block of control logic coupled to the memory, the block of control logic to write the plurality of data to the plurality of configuration registers according to the plurality of address information (see 205, Fig. 2; for multiple logic blocks which control the loading).
- The non-volatile memory is an Electrically Erasable Programmable Read-only Memory (See Col. 3, line 43) and
- the non-volatile memory has a memory size less than a memory size sufficient to fill all the configuration registers (the memory segment 0-5n storing the information stores values for only some (less than all) configuration registers; see Col. 3, lines 10-15; Claim 2)

43. Kao does not expressly teach that the device is an Ethernet controller device, instead teaching a PCI/ISA bus bridge.

44. Cohen teaches a similar system for loading configuration registers of a PCI/peripheral bus interface (24, Fig. 2) from a non-volatile memory (12D, Fig. 2). Cohen teaches that the PCI bus bridge may be used to interface different devices to the bus, such as an Ethernet device or a SCSI interface (Col. 2, lines 6-10).

45. At the time of the present invention it would have been obvious to one of ordinary skill in the art to modify the system of Kao by using it in an Ethernet controller device.

46. The motivation for doing so is taught by Cohen, in Col. 2, lines 6-28, namely that different devices that use a PCI bus use different configuration register settings. It may be possible to reuse the bus interface chip if the configuration settings are reprogrammable; therefore, the system to load the registers froma reprogrammable memory is used.

47. A further motivation is found in Bonaccio, which also teaches a similar system for loading configuration registers from an EEPROM. Bonaccio teaches in Par. 4 that using programmable registers is widely used in many ICs to allow the user to configure the function of the chip. Further, in Pars. 20-21, he teaches that the methods of loading configuration registers (which are similar to those of the present invention) may be applied not only to ICs such as hard disk channel controllers, but to any IC configured by registers.

48. Therefore, one of ordinary skill would be motivated to use the system of Kao in an Ethernet device as does Cohen, thereby obtaining the invention of claims 20-21.

49. **Claims 14 and 17-19 are rejected under 35 USC § 103(a) as being unpatentable over Kao and Bonaccio as applied to claim11, and further in view of Tomashima, US 6,480,946.**

50. **As for claim 14,** Kao and Bonaccio teach the limitations of claim 11 as above. However, Kao and Bonaccio do not teach that the loading occurs during a memory design validation stage.

51. However, Tomishima teaches a memory timing validation system which is used to determine the optimum settings for a memory.

52. At the time of the invention it would have been obvious to perform the method of Kao and Bonaccio during a stage of memory design validation. As noted by Fig. 43 and Cols. 37-38 of Tomashima, different values for timing, voltage can be successively loaded into the registers to see which are the optimum ones. This method would be advantageous in the system of Kao and Bonaccio, for the same reason as that of Tomashima. In that system, different placements of memory chips create different skew values which require different configuration settings. These problems also plague systems such as that of Kao and Bonaccio. Therefore, the method of Tomshima would be beneficial in discovering the optimum settings during a memory design validation stage.

53. **As for claim 17,** Kao and Bonaccio teach the limitations of claim 11 as above. However, Kao and Bonaccio do not teach: generating a desired information associated with the desired configuration, wherein generating comprises: if there exists at least one of the plurality of test data corresponding to one of the plurality of registers having

default data values equal to desired data for achieving the desired configuration prior to loading, then storing subsequent test information and repeating c), d), and e) using the subsequent test information; else identifying the desired information to be the test information.

54. Tomashima teaches a system and method for determining desired configuration values. In this system, default timing configuration values are loaded, and the system is tested (Col. 37, lines 1-12). If the results are unsatisfactory, timing delays are added. If, however, the results are satisfactory and the default timing values are correct but the voltage is not at the maximum, voltage values are adjusted and the test is repeated.

55. At the time of the invention it would have been obvious to apply this multi-stage testing of Tomashima to the system of Bonaccio and Kao. This would have been obvious because even if, for instance, some default configuration values are correct, others may not be. I.e., if one bus timing value is correct, a voltage value may not be. Therefore, a multi-stage testing process to determine the correct/optimal values (as shown in Fig. 43 and Col. 37) would be advantageous.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse Diller whose telephone number is (571) 272-4173. The examiner can normally be reached on 9:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JD

Brian R. Peugh
Primary Examiner